REMARKS

Claims 6, 13, and 26 are cancelled herein. Thus, claims 1-5, 7-12, 14-25 and 27 are all the claims presently pending in the application. All of the pending claims stand rejected on prior art grounds, under 35 U.S.C. §103(a). Claims 1, 8, 15, and 21 stand rejected under 35 U.S.C. §112, first paragraph. Claims 21-27 stand rejected under 35 U.S.C. §101. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The 35 U.S.C. §112, First Paragraph, Rejection

The Office Action indicates that claims 1, 8, 15 and 21 stand rejected under 35 U.S.C. §112, first paragraph, because "the claim(s) contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant are that the inventors(s) at the time the application was filed, had possession of the claimed invention." Specifically, the Examiner is unable to determine wherein in the specification it discloses the feature of "creating, in a database, models from the regression analysis only showing a relationship between said historical gate dimensions" or the feature of "a regression analyzer adapted to determine relationships between historical critical gate dimensions."

As disclosed in the specification at paragraphs [0019] and [0021], a regression analysis is performed by treating the critical gate dimension as the independent variable and the costs as the dependent variable to produce relationship curves (as illustrated in

FIG. 1) (i.e., as discussed in paragraph [0024], the output of the regression analysis is relationship curves of FIG. 1). Paragraph [0038] further clarifies that a regression analyzer performs the regression analysis (i.e., performs a least-square analysis) on the historical data (i.e., the historical costs and historical critical gate dimensions) from the different technologies to create the critical dimensions/cost relationships (i.e., the relationship curves of FIG. 1).

Therefore, to better clarify the features of the invention, claims 1 is amended herein to include the feature that computer is adapted to "perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs". Similarly, claims 8 and 21 are amended herein to include the feature of "performing a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that show only relationships between said historical critical gate dimensions and said historical costs". Finally, claim 15 is amended herein to include the feature of "a regression analyzer adapted to produce relationship curves that show relationships between historical critical gate dimensions and historical costs of different technologies run at said fabricator".

In view of the foregoing, the Examiner the use respectfully requested to reconsider and withdraw this rejection.

II. The 35 U.S.C. §101 Rejection

Claims 21-27 stand rejected under 35 U.S.C 101. Independent claim 21 has been amended, above, to overcome this rejection. Support for this amendment is found in paragraph [0040] of the specification.

III. The Prior Art Rejections

Claims 1-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "21st Century Semiconductor Manufacturing Capabilities", hereinafter referred to as "Manufacturing" in view of Evans et al. (U.S. Patent No. 6,775,647), hereinafter referred to as Evans. Applicants respectfully traverse these rejections because the Office Action fails to establish a prima facie case of obviousness under MPEP§2141-2143. Specifically, the prior art references cited refer to non-analagous prior art; there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings; and the cited prior art references combined fail to teach or suggest all of the claim limitations.

1. **Non-Analagous Art**

The Applicants submit that neither Manufacturing, nor Evans represent analagous art as required by MPEP §2141. Specifically, it is well known that "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicants endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." (See *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992).

(a) Manufacturing is not an analogous prior art. More specifically, Manufacturing is a paper that broadly discusses responses of semiconductor industry management and university faculty to the predictions of Moore's Second Law, which states that one of the challenges of Moore's First Law (i.e., semiconductor device complexity doubles every 18 months) is that facility costs increase on a semi-log scale (see Abstract). It does not disclose any specific method or system, much less a method or system of predicting the cost for developing new semiconductor products. Figures 1-3 and Tables 1-3 of Manufacturing illustrate data related to Moore's First and Second Laws within the entire semiconductor industry. That is, Figure 1 illustrates Moore's First Law. Figure 2 illustrates that high volume device manufacturing resulting from Moore's First Law has lead a reduction in a cost per chip between 1980 and 2010. Table 1 illustrates that programs associated with Moore's First Law have consequences (e.g., consequences related to feature sizes reduction, chip sizes increases, wafer diameter, yield, etc.). Figure 3 further illustrates cost trends related to Moore's First Law (i.e., illustrates Moore's Second Law). Table 2 is the same as Table 1 but further illustrates the addition of equipment costs and operational efficiency associated with Moore's First Law. Manufacturing thus recognizes two problems with regard to the semiconductor manufacturing industry and, specifically, to cost per chip element and factory cost containment: (1) programs that lower cost per element can add to factory cost; and (2) some programs have diminishing returns. However, while Manufacturing deals with responses of semiconductor industry management to the predictions of Moore's Law, no where in Manufacturing are a system and method for actually predicting new semiconductor product costs at a fabricator disclosed. Rather the cited portions simply

refer to data collected throughout the industry over time as it relates to Moore's Laws and to statistical projections made based on that data in light of Moore's Laws. Consequently, the Applicants disagree with the Examiner's assertion that Manufacturing relates to a "field of endeavor of predicting a cost for developing new products" at a fabricator.

(b) Evan is also not an analogous prior art. The Office Action notes that Manufacturing does not expressly disclose performing a regression analysis on historical costs of historical critical gate dimensions. To cure this deficiency, the Office Action refers to Evans for teaching a method of estimating manufacturing costs using a regression analysis. While Evans discloses a method and system for estimating manufacturing cost of aircraft engines using regression analysis on individual components, the estimation of manufacturing cost of aircraft engines is not "reasonably pertinent to the particular problem with which the inventor is concerned, namely predicting new semiconductor product costs.

More specifically, as mentioned above and stated in the Abstract of Manufacturing, the semiconductor industry, unlike other industries generally adheres to Moore's Laws (i.e., device complexity doubles about every 18 months and facility costs increase on a semi-log scale). Thus, methods of cost predictions in other manufacturing industries, such as aircraft manufacturing industries, would not be reasonably pertinent to cost predictions methods in the semiconductor manufacturing industries.

Additionally, it would not be reasonable for an individual interested in predicting costs for a new semiconductor design to look to different manufacturing industries because of the nature of the specific components of semiconductor products.

Specifically, "gate dimensions" have an effect on "semiconductor product costs" which is unique to the semiconductor manufacturing industry and which would not benefit from the teachings found within non-semiconductor manufacturing industries, such as the aircraft engine manufacturing, where costs typically do not increase exponentially with the decreasing dimension of a particular component. For example, there are many sizes and dimensions associated with the various components of a semiconductor device (e.g., the size and thickness of the source and drain regions, the size and depth of the channel region, the size and thickness of the gate oxide, sizes and positions spacers adjacent the gate, sizes and dimensions of various insulators and contacts connected to the source, drain, and gain regions, gate dimensions, etc.). However, because of a significant inverse cost/gate dimension relationship, the claimed invention is able to predict the product costs of a new semiconductor device based on a new gate dimension alone without having to analyze the sizes/dimensions associated with these other elements of the device.

Other manufacturing industries, e.g., such as the aircraft manufacturing industry discussed in Evans, do not contain a component that exhibits such a significant inverse cost/size relationship. For example, Evans discloses a regression analysis to establish a relationship between specific part features and multiple different processing costs related to achieving those features (see step 35 of Figure 2). However, the cited portions (column 5, lines 18-50) of Evans describe developing a cost model for a family of parts in an aircraft engine (e.g., a guide vane/diffuser family). The model is defined by the alternate designs for the guide vane and the different configurations and material applications for each design. Then, manufacturing costs for each of the three

configuration of each of the two design variation in the three material selections (i.e., 18 points) are estimated based on the processes used to manufacture the part (see col. 5, line 65-col. 6, line 2). For example, to determine the cost of manufacturing each design/configuration variation for the part, the cost of processing is estimated (e.g., both the cost of casting the part (see col. 6, lines 8-18) and then the cost of deburring that part are considered). To determine the cost of a deburring operation, input parameters such as the diameter to deburr, the number of diameters to debur and the part size (i.e., height, weight and length) are considered (see col. 7, lines 3-10). Thus, the greater the size of the part, the more deburring required which would necessarily result in an increased cost in the cost of building that component (i.e., there is a direct relationship between the cost of the component and the size component).

A cost model for the family of parts is then built using a regression analysis based on the 18 points (col. 7, line 19). Then, resource data, including the cost model algorithms for each family of parts, are gathered for the designing and cost estimation of a complete engine. That is, the user can select specific part designs and configurations for each sub-component that is to be incorporated into the engine in order to then estimate the cost of the engine as a whole (see col. 7, line 61-col. 8, line 65; Abstract).

Therefore, there is no inverse relationship between the cost of a single component and its size, much less an inverse relationship between the cost of the entire product and the size of a single component within the product. Thus, a reference to an aircraft manufacturing industry cost prediction method could not be considered reasonably pertinent to the particular problem with which the inventor was concerned (i.e., cost predictions for a semiconductor product at a fabricator based on gate dimension).

2. **Lack of Motivation to Combine Manufacturing and Evans.**

The Examiner asserts that the "motivation is in the reference (see Evans; col. 3, lines 7-34 and col. 5, lines 19-39) and is reasonably pertinent to the particular problem with which the applicant is concerned." The Office Action further asserts on page 2 that the "motivation is in the reference (see Evans; col. 3, lines 7-34 and col. 5, lines 19-39) and is reasonably pertinent to the particular problem with which the applicant is concerned." More specifically, the Office actions provides on page 5 that "Since Evans et al. and Manufacturing are both from the same field of endeavor of predicting a cost for developing new products, the purpose disclosed by Evans et al. would have been well recognized in the pertinent field of Manufacturing. Accordingly, it would have been obvious at the time of the invention was made to a person having ordinary skill in the ad to modify the invention of Manufacturing such that the invention performs a regression analysis …" The Applicants respectfully disagree because Evan relates to estimating costs within the field of aircraft engines, whereas the cited portions of Manufacturing refer statistical projections made based on industry-wide data collected over time in light of Moore's Laws, which apply specifically to the semiconductor manufacturing industry.

More specifically, as discussed in detail above, the paper of Manufacturing "discusses the technological responses of industry management and university faculty to the predictions of Moore's Second Law", which is specific to the semiconductor manufacturing industry. Since the problems addressed in Manufacturing, namely, Moore's Laws, are specific to the semiconductor manufacturing industry, there would be no reason or motivation to combine the teachings of Manufacturing with a method related

to manufacturing costs in a completely different industry (e.g., the aircraft manufacturing industry referred to in Evans).

3. <u>Manufacturing and Evans fail to disclose each and every limitation of the claims</u>.

The proposed combination of Manufacturing and Evans fails to teach each and every element of the claimed invention. Specifically, the cited prior art references fail to the following features of amended independent claim 1 or the similar features found in amended independent claims 8, 15 and 21: (1) "a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator"; (2) "perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs"; and (3) "predict product costs of said new device based on said user inputs and said relationship curves".

Specifically, the Office Action cites Manufacturing generally as disclosing: (1) a system and method for **predicting semiconductor product costs at a fabricator**; (2) "a storage medium including a database of historical critical gate dimensions and historical critical ground rules correlated to cost functions at said fabricator (page 1, FIGS. 2-3: Tables 1-3)"; (3) "receive said user inputs (see especially Figs. 2-3, Tables 1-3 and Supra Response to Applicant's Argument)"; (4) "relationship between said historical critical gate dimensions and said historical costs (see Supra Figs. And Tables)"; and (5) "input new design parameters and new critical gate dimensions of a new device into the database and predicting product costs of the new device based on the modes (see the

entirety of the document, to note how "Operational modeling and simulation" and "Knowledge Management" work to compute the costs for the new design)." The Examiner further acknowledges that Manufacturing fails to disclose a regression analysis on historical costs of historical critical gate dimensions at a specific fabricator and then uses the historical critical gate dimensions as independent variables and the historical costs as dependent variables in order to produce models as recited in the claims. Thus, the Examiner cites col. 5, lines 19-38 of Evans as teaching this feature. The Applicants respectfully disagree.

As discussed above, Manufacturing is a paper that discusses "responses of industry management and university faculty to the predictions of Moore's Second Law", which states that one of the challenges of Moore's First Law (i.e., device complexity doubles every 18 months) is that facility costs increase on a semi-log scale (see Abstract). Figures 1-3 and Tables 1-3 illustrates data related to Moore's First and Second Laws within the entire semiconductor industry. That is, Figure 1 illustrates Moore's First Law. Figure 2 illustrates that high volume device manufacturing resulting from Moore's First Law has lead a reduction in a cost per chip between 1980 and 2010. Table 1 illustrates that programs associated with Moore's First Law have consequences (e.g., consequences related to feature size reduction, chip size increases, wafer diameter, yield, etc.). Figure 3 further illustrates cost trends related to Moore's First Law (i.e., illustrates Moore's Second Law). Table 2 is the same as Table 1 but further illustrates the addition of equipment cost and operational efficiency associated with Moore's First Law. Manufacturing thus recognizes to problems with regard to cost per chip element and

factory cost containment: (1) programs that lower cost per element can add to factory cost; and (2) some programs have diminishing returns.

No where in the cited portions of Manufacturing are a system and method for predicting semiconductor product costs at a fabricator disclosed. Rather the cited portions simply refer to data collected in the industry over time as it relates to Moore's Laws and with statistical projections based on Moore's Laws and operational modeling without reference to cost predictions.

No where in Manufacturing does it teach or disclose "a storage medium including a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator." The pages, figures and tables cited refer to relative chip complexity, average feature size reduction, average chip size reduction, average wafer diameter, relative operational efficiency, relative equipment cost, etc., from year to year (e.g., resulting from factory cost control programs (see table 2)) with predictions for future year(s). They do not disclose a storage medium that includes a database of historical costs and historical critical gate dimensions of different technologies run at a fabricator.

No where in Manufacturing does it teach or disclose "receive said user inputs", where user inputs are "for new design and new critical gate dimensions associated with a new device to be produced at said fabricator". Again, the cited figures and tables refer to relative chip complexity, average feature size reduction, average chip size reduction, average wafer diameter, relative operational efficiency, relative equipment cost, etc., from year to year with a prediction for future year(s). They do not disclose inputting a

new design and new critical gate dimensions associated with the new device to be produced at the fabricator.

No where in Manufacturing does it teach or disclose a "relationship between said historical critical gate dimensions and said historical costs." Again, the cited figures and tables refer to relative chip complexity, average feature size reduction, average chip size reduction, average wafer diameter, relative operational efficiency, equipment costs, etc., from year to year with a prediction for future year(s). They do not disclose actual historical feature sizes, much less actual gate dimensions and a relationship between these actual historical gate dimensions and costs of the product itself.

No where in Manufacturing does it disclose "input new design parameters and new critical gate dimensions of a new device into the database and predicting product costs of the new device based on the models". The Examiner indicates that this feature is disclosed in "the entirety of the document, to note how "Operational modeling and simulation" and "Knowledge Management" work to compute the costs for the new design). 37 C.F.R. §1.104(c)(2) provides that "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." Given the nature of the Manufacturing paper, the citation of the Examiner does not sufficiently designate the particular part of Manufacturing relied upon by the Examiner to teach this feature. Furthermore, the "Application of OM&S Technology" section of the Manufacturing paper does not disclose the claimed features of

"inputting new design parameters and new critical gate dimensions of a new device into said database; and predicting product costs of said new device based on said relationship curves." That is, the cited portions of Manufacturing discusses generally applications of operational modeling, without reference at all to cost predictions for a new device based on relationship curves that only show relationships between said historical critical gate dimensions and said historical costs.

Finally, no where in the cited portions of Evans does it teach or disclose "performing a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that show only relationships between said historical critical gate dimensions and said historical costs". Evans discloses predicting cost based on actual dimensions of materials of a finished piece in an aircraft not the historical dimensions of a specific component and historical costs of the engine. Specifically, Evans requires that the dimensions of each part needs to be specified in the regression analysis (see column 2, lines 19-34 and column 5, lines 19-39 of Evans). The regression analysis establishes a relationship between specific part features and multiple different processing costs related to achieving those features (see step 35 of Figure 2). As discussed in detail above, the cited portions (column 5, lines 18-50) of Evans describe developing a cost model for a family of parts in an aircraft engine (e.g., a guide vane/diffuser family). The model is defined by the alternate designs for the family of parts and the different configurations and material applications for each design. Then, manufacturing costs (i.e., a cost model) for each of the configurations/designs is estimated based on the processes used to manufacture the part using a regression analysis.

Then, resource data, including the cost model algorithms for each family of parts, are gathered for the designing and cost estimation of a complete engine. That is, the user can select specific part designs and configurations for each sub-component that is to be incorporated into the engine in order to then estimate the cost of the engine as a whole (see col. 7, line 61-col. 8, line 65; Abstract). Therefore, if Evans' teaching were translated into semiconductor manufacturing processes, Evans would require that the size and dimensions of each component of the semiconductor product (i.e., the gates, gate oxides, sources, drains, channels, contacts, etc.) all be specified as well as the associated costs in order to arrive at a future cost prediction for the entire completed new product. Therefore, even if the teachings of Evans were applied to semiconductor manufacturing processes, Evans still would not teach or suggest to one ordinarily skilled in the art a system and method for predicting new product costs of semiconductor products based only on the critical gate dimension (as claimed).

Moreover, because Evans is rooted in the technology of manufacturing aircraft engines, it does not discuss the relationship between historical critical gate dimensions and historical costs (nor would it be expected to). There simply is no teaching for the claimed invention which provides the benefit of allowing the user to input only the gate dimensions to achieve a prediction of future costs for entire semiconductor products. There are many different dimensions within semiconductor devices such as the size and thickness of the source and drain regions, the size and depth of the channel region, the size and thickness of the gate oxide, sizes and positions of spacers adjacent the gate, sizes and dimensions of various contacts and insulators connected to the source, and drain, and gain regions. The claimed invention is able to predict the product costs of new

semiconductor devices simply by specifying a new gate dimension, without having to specify dimensions, sizes, locations, thickness of any other elements such as source, drain, gate oxide, contacts, channel region, etc. To equate the claimed ability to predict costs into an aircraft engine industry manufacturing process would require a teaching of predicting the cost an airplane based on, for example, the diameter of a part of the engine. Evans clearly does not provide such teaching.

Additionally, Applicants note that even if one ordinarily skilled in the semiconductor product cost estimating field had made reference to Evans, the proposed combination of references still would not teach or suggest that the regression analysis should be limited only to historical critical gate dimensions as is required by independent claims 8, 15, and 21. As shown in the previous discussion, the Manufacturing reference does not discuss calculating future costs based upon historical critical gate dimensions. Instead, the Manufacturing reference only makes forecasts of chip complexity, cost per chip element set, yield percentage, etc. Evans only discusses the manufacturing of aircraft engines and is completely silent regarding any aspects of semiconductor manufacturing. Therefore, Evans also omits any teaching of limiting the regression analysis to critical gate dimensions.

Therefore, it is Applicants' position that the Manufacturing paper, even if combined with Evans, does not teach or suggest the following features of amended independent claim 1 or the similar features found in amended independent claims 8, 15 and 21: (1) "a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator"; (2) "perform a regression analysis on said historical costs and said historical critical gate dimensions, using said historical critical

gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs"; and (3) "predict product costs of said new device based on said user inputs and said relationship curves".

Therefore, amended independent claims 1, 8, 15 and 21 are patentable over "Manufacturing" in view of Evans. Further, dependent claims 2-5, 7, 9-12, 14, 16-20, 22-25 and 27 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, Applicants submit that claims 1-5, 7-12, 14-25 and 27, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456

Respectfully submitted,

Date: ___03-01-07____ _____\Pamela M. Riley__________________

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